Amendments to the Specification:

The following amendments to the specification correct typographical errors and contain no new matter within the purview of 35 U.S.C. § 132(a).

Please replace paragraph 30 with the following paragraph:

[0030] FIG. 3 is a block diagram of the decoder 140 of FIG. 1. As shown in FIG. 3, the decoder 140 includes a pre-processor 310, a tone-detector 312, a Finite-Impulse-Response (FIR) filter 314, an Automatic Gain Control (AGC) device 316, an Interpolate Timing Recovery (ITR) device 318, a PR4 channel decoder 320, a sync detector 322, an un-shuffler 324, a LDPC decoder 326 and an RLL decoder 328. While the exemplary decoder 140 is implemented using various VLSI logic circuits, it should be appreciated that the various devices 3023 10-328 can be implemented using any combination of signal processing hardware, sequential instruction devices and dedicated logic, without departing from the spirit and scope of the present invention.